Solution to the Most Important DLD Problems shown in the Previous Video

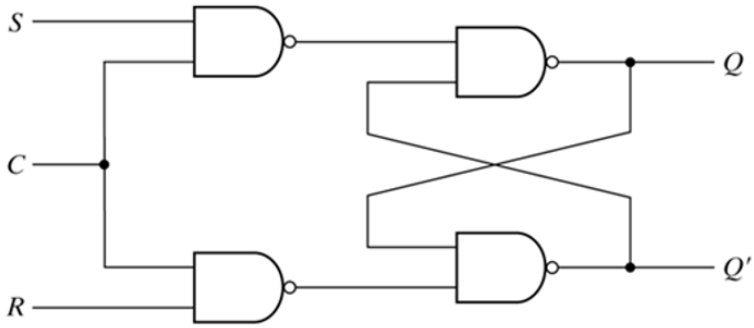
Problem # 01: What is Gated SR Latch? Or it circuit diagram maybe given, complete the truth table of SR latch. Is there any specific input combination for which we have an invalid output? If there, how can we get rid of this?

A **Gated SR Latch** (also called a **Clocked SR Latch** or **Enabled SR Latch**) is a basic digital memory circuit that stores **1 bit of data** and works only when an **Enable (or Clock) signal** is active.

It is an improved version of the simple **SR Latch** because the inputs are controlled by an additional signal called **Enable (E)** or **Clock (CLK)**.

Part a: **[3+2]**

i. Complete the characteristic table for the **SR latch** shown below:



C	S	R	Q	Q'
0	X	X	no	Change
1	0	0		4
1	0	1	0	1
1	1	0	1	0
1	1	1	Indeterminate.	

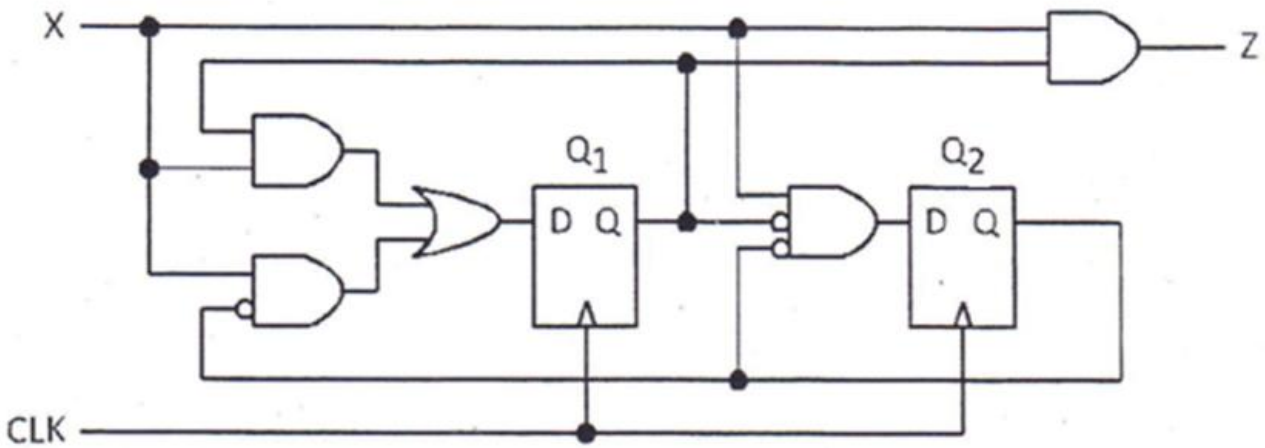
ii. How the indeterminate state problem can be resolved completely?

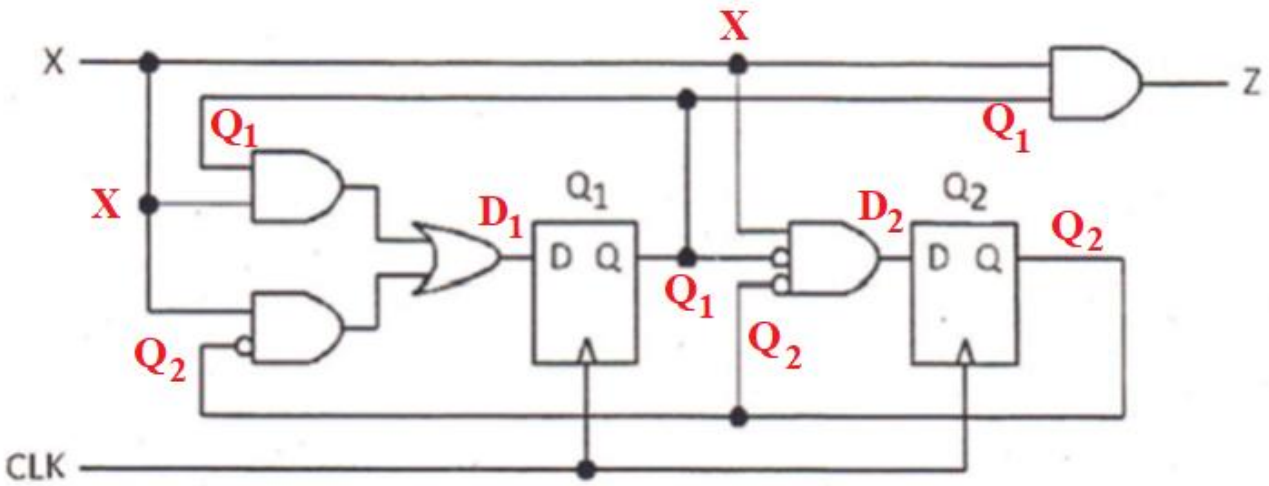
Make sure that both inputs S and R never equal 1. This can be done by connecting both inputs say 'D'. The input 'D' is connected directly to the 'S' input while its complement is applied to the 'R' input.

Problem # 02

For the following clocked sequential circuit with one input (X) and one output (Z):

1. Drive a state table and draw a state diagram for the circuit.
2. Redesign this circuit by replacing the Q1 flip-flop (i.e. the D flip-flop holding Q1 state) with a JK flipflop, and the Q2 flip-flop with a T flip-flop. Only show the excitation equations (or state equations) for J1, K1, and T2.





Let the present states of the two D flip-flops be $Q_1$and Q_2.

From the circuit:

1) State Equations

For Q_1

The input of the first D flip-flop is obtained from two AND gates followed by an OR gate.

$$D_1 = XQ_1 + X\bar{Q_2}$$

Hence,

$$Q_1^+ = XQ_1 + X\bar{Q_2}$$

For Q_2

The second D flip-flop input comes from a gated AND structure:

$$D_2 = X\bar{Q_1}\,\bar{Q_2}$$

Hence,

$$Q_2^+ = X\bar{Q_1}\,\bar{Q_2}$$

Output Equation

The output gate is an AND gate:

$$Z = XQ_1$$

---

2) State Table

Present state $= (Q_1Q_2)$

Next state $= (Q_1^+Q_2^+)$

Present State (Q_1Q_2)	Input (X)	Next State $(Q_1^+Q_2^+)$	Output (Z)
00	0	00	0
00	1	11	0
01	0	00	0
01	1	00	0
10	0	00	0
10	1	10	1
11	0	00	0
11	1	10	1

---

3) State Diagram

Since the output depends on both **state** and **input** ($Z = XQ_1$), this is a **Mealy Machine**.

So, labels are written as:

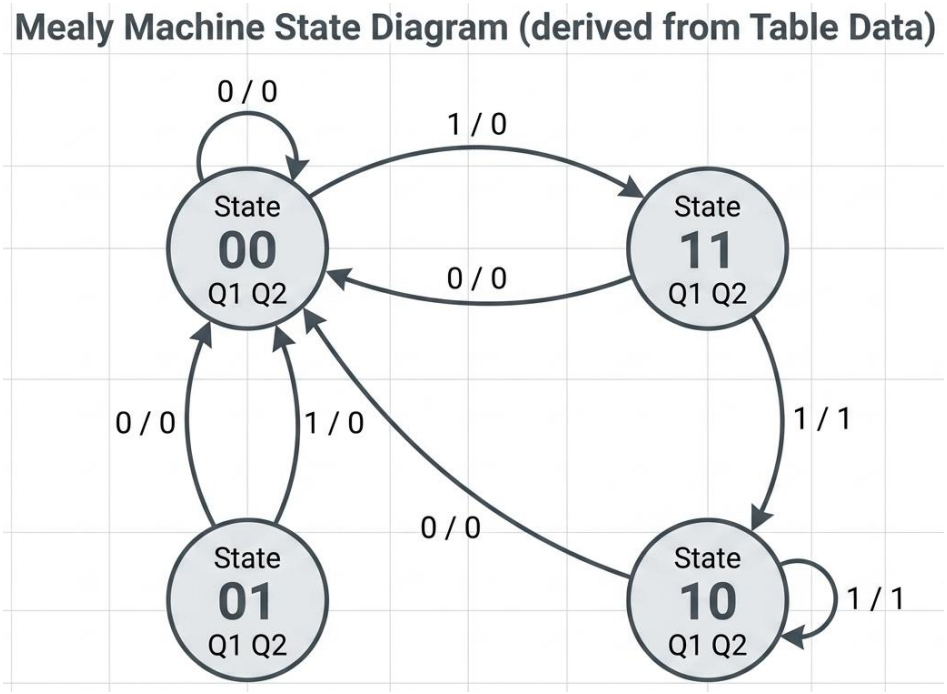
$$X/Z$$

meaning:

Input/Output

States

$$S_0 = 00, S_1 = 01, S_2 = 10, S_3 = 11$$

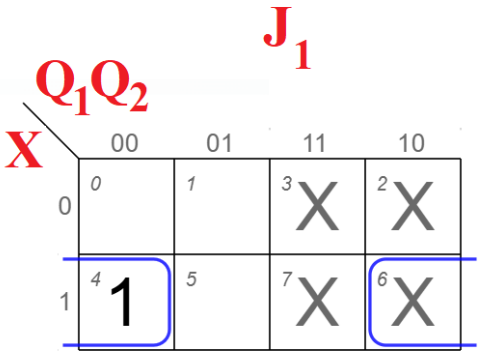


4) Redesign Using JK and T Flip-Flops

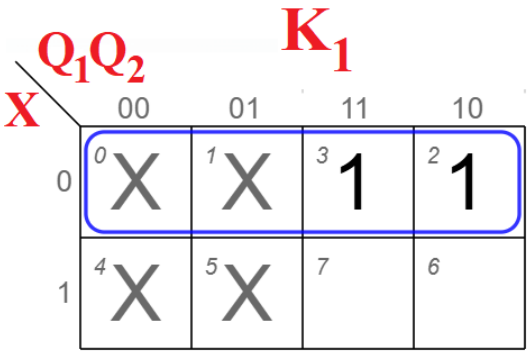
We replace:

- Q_1 flip-flop → JK flip-flop
- Q_2 flip-flop → T flip-flop

Present State (Q_1Q_2)	Input (X)	Next State ($Q_1^+Q_2^+$)	Output (Z)	J_1	K_1	T_2
00	0	00	0	0	X	0
00	1	11	0	1	X	1
01	0	00	0	0	X	1
01	1	00	0	0	X	1
10	0	00	0	X	1	0
10	1	10	1	X	0	0
11	0	00	0	X	1	1
11	1	10	1	X	0	1



$J_1 = X\overline{Q}_2$

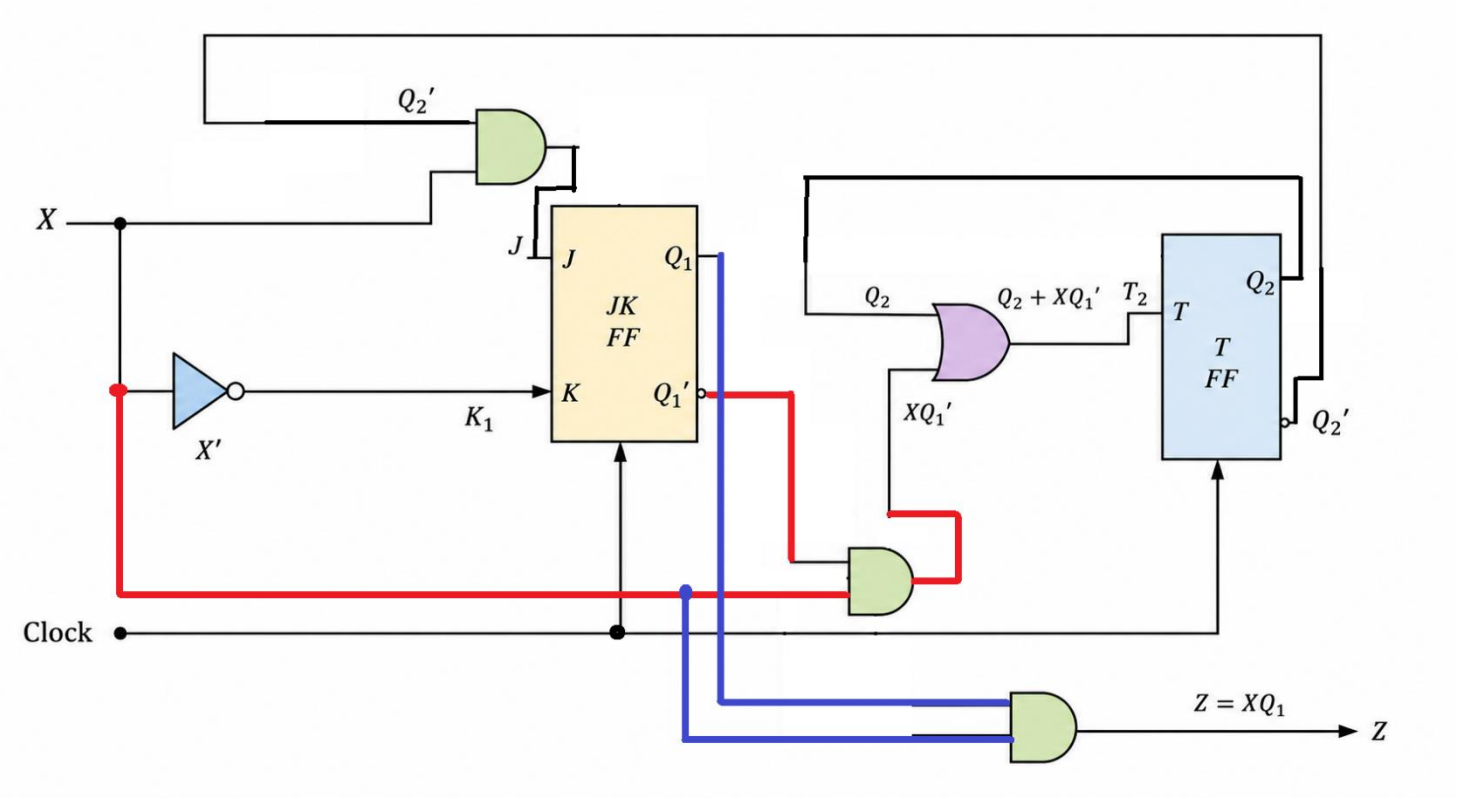


$K_1 = \overline{X}$

T_2

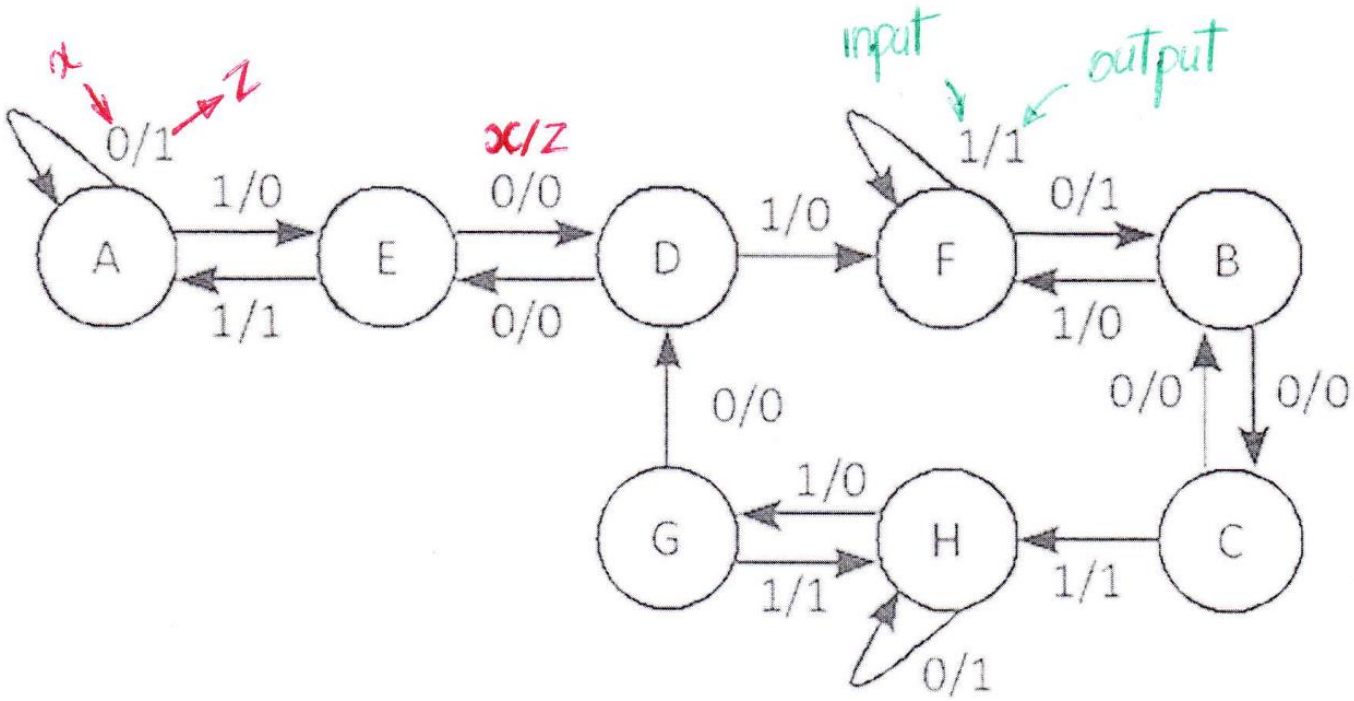
XQ_1Q_2	00	01	11	10
0	0	1 1	3 1	2 X
1	4 1	5 1	7 1	6

$$T_2 = Q_2 + X\bar{Q}_1$$



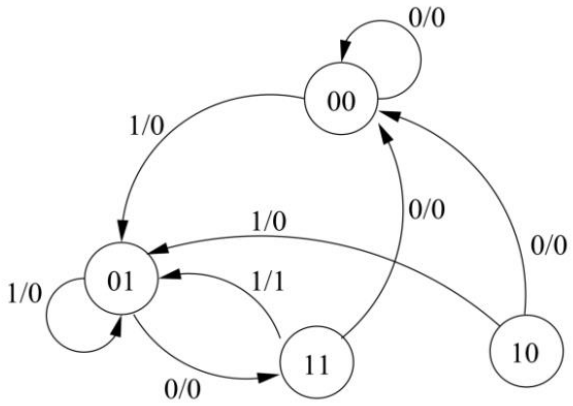
Problem # 03: Draw the state diagram for the table below that describes a finite-state machine which has one input x and one output z.

This is a Mealy Model as output depends on the present state and the input (x) that is $Output = f(Present\ State, input)$



Problem # 04:

Consider the following state diagram for a synchronous circuit with one input X and one output Z. Analyze this state diagram and draw its circuit implementation using JK flip-flop (state Q0) and T flip-flop (state Q1) and MUX-4x1 for Z.



PS (Q_1Q_0)	Input (X)	NS $(Q_1^+Q_0^+)$	Output (Z)
00	0	00	0
00	1	01	0
01	0	11	0
01	1	01	0
10	0	00	0
10	1	01	0
11	0	00	0
11	1	01	1

$$Z = Q_1Q_oX$$

Excitation Table of JK & T Flip Flop

INPUT		OUTPUT	
Qn	Q(n+1)	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Q_t	Q(t+1)	T
0	0	0
1	0	1
0	1	1
1	1	0

PS (Q_1Q_0)	Input (X)	NS $(Q_1^+Q_0^+)$	Output (Z)	J_0	K_0	T_1
00	0	00	0	0	X	0
00	1	01	0	1	X	0
01	0	11	0	X	0	1
01	1	01	0	X	0	0
10	0	00	0	0	X	1
10	1	01	0	1	X	1
11	0	00	0	X	1	1
11	1	01	1	X	0	1

For J_0

Q_1 \ Q_0X	00	01	11	10
0	0	1 1	3 X	2 X
1	4	5 X	7 X	6 X

$$J_0 = X$$

For K_0

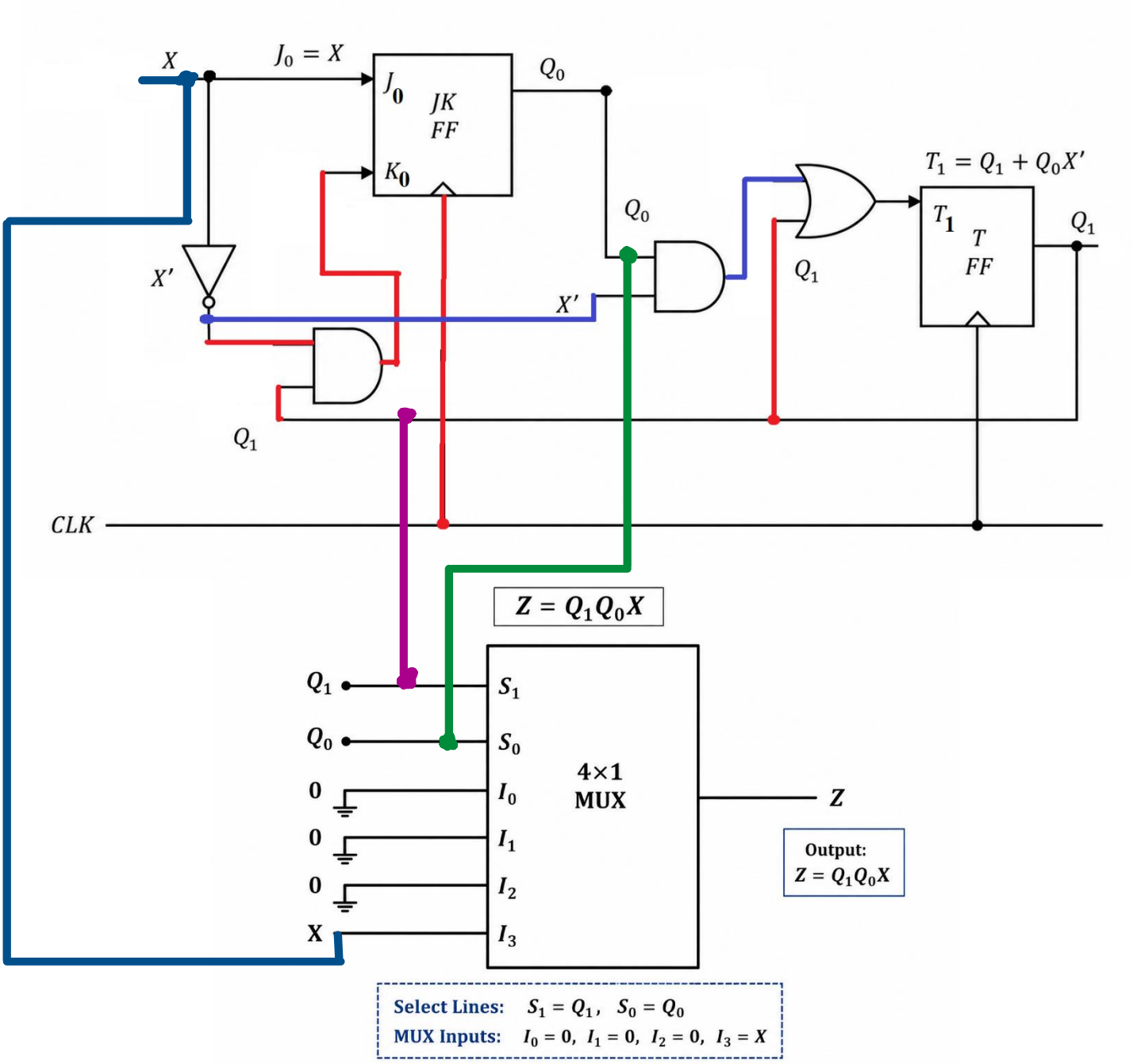
Q_1 \ Q_0X	00	01	11	10
0	0 X	1 X	3	2
1	4 X	5 X	7	6 1

$$K_0 = Q_1\bar{X}$$

For T_1

Q_1 \ Q_0X	00	01	11	10
0	0	1	3	2 1
1	4 1	5 1	7 1	6 1

$$T_1 = Q_1 + Q_0\bar{X}$$


X
$J_0 = X$
J_0
JK
FF
K_0
Q_0
$T_1 = Q_1 + Q_0X'$
T_1
T
FF
Q_1
Q_0
Q_1
X'
X'
Q_1
CLK
$Z = Q_1Q_0X$
Q_1
Q_0
0
0
0
X
S_1
S_0
I_0
I_1
I_2
I_3
4×1
MUX
Z
Output:
$Z = Q_1Q_0X$
Select Lines: $S_1 = Q_1$, $S_0 = Q_0$
MUX Inputs: $I_0 = 0$, $I_1 = 0$, $I_2 = 0$, $I_3 = X$

Problem # 05

Design a digital circuit that takes two 4-bit numbers A and B as input and generates output Z as follows:

- If A and B are odd numbers then Z=A-B
- If A and B are even numbers then Z=B-A
- If A is an even number and B is an odd number then Z=A+B
- If A is an odd number and B is an even number then Z=A-B-1

Assume that you have access to as many as you need of AND, OR, INV, XOR gates and only one FULL-ADDER, DECODER and MULTIPLEXER of any size.

Sol:- I/Ps: A & B. O/P: Z

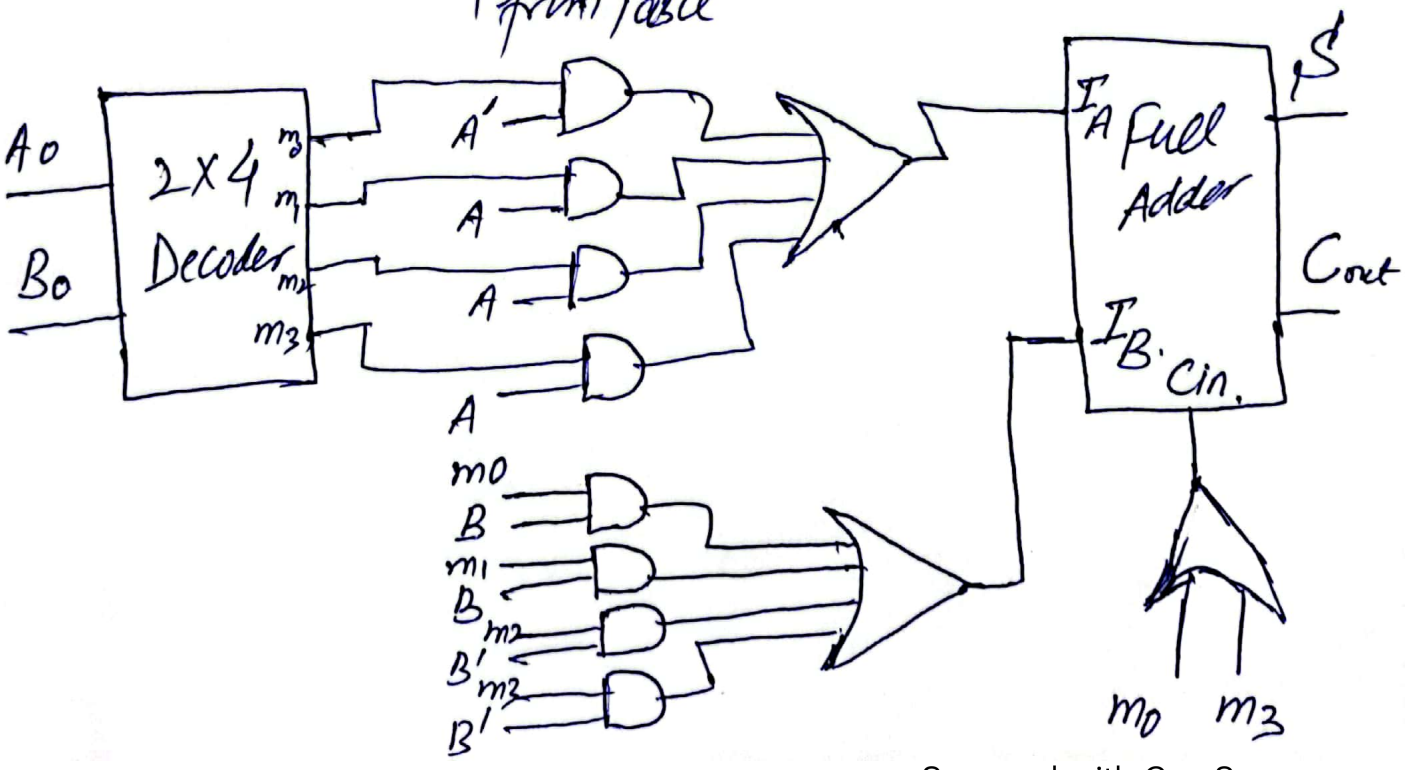
$A = A_3 A_2 A_1 A_0$

$B = B_3 B_2 B_1 B_0$

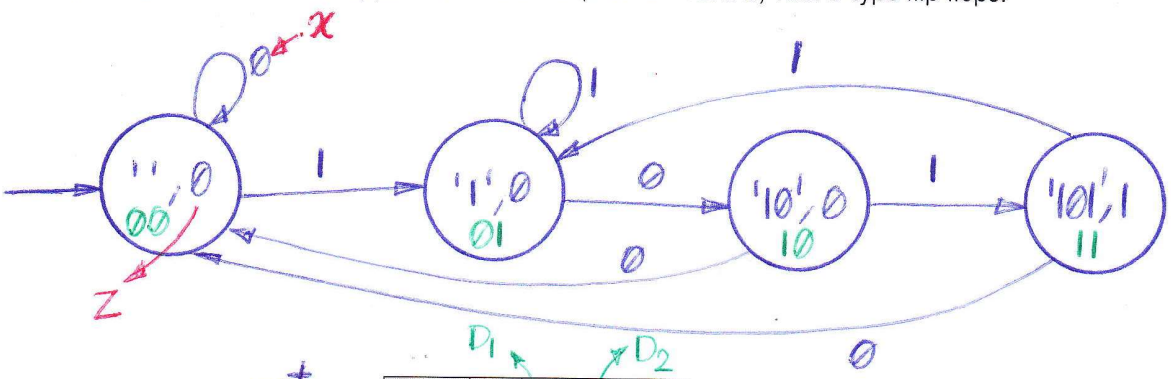
Function Table:-

	Enabled A_0 B_0	function Z	Full Adder Inputs. I_A	I_B	Cin.
m_0	0 0	B-A	A'	B	1
m_1	0 1	A+B	A	B	0
m_2	1 0	A-B-1	A	B'	0
m_3	1 1	A-B	A	B'	1

Eqn. of Cin = $m_0 + m_3$ from table



[Q4] Draw a logic diagram for non-overlapped '101' detector (Moore machine) with D-type flip-flops.



D_1 D_2

PS q_1q_2	IN x	NS q_1q_2	OUT z
00	0	00	0
00	1	01	0
01	0	10	0
01	1	01	0
10	0	00	0
10	1	11	1
11	0	00	0
11	1	01	0

CS^+

Moore: $OUT = f(NS)$

Mealy: $OUT = f(CS, IN)$

$$z = \begin{cases} q_1q_2 & \text{Moore } ① \\ q_1q_2'x & \text{Mealy } ② \end{cases}$$

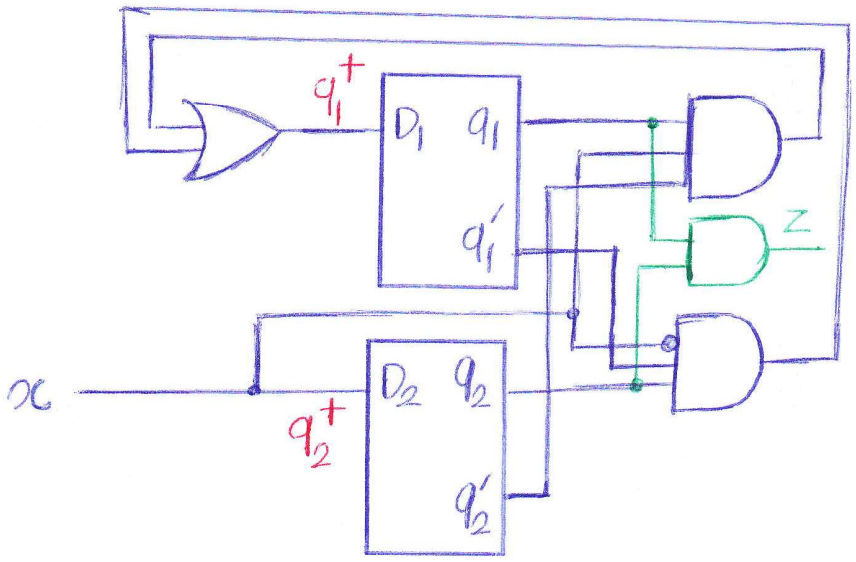
q_1

x \ q_1q_2	00	01	11	10
0	0	(1)	0	0
1	0	0	0	(1)

q_2

x \ q_1q_2	00	01	11	10
0	0	0	0	0
1	1	1	1	1

$D_1 = q_1^+ = xq_1'q_2 + xq_1q_2'$ $\quad D_2 = q_2^+ = x$



example

overlap

$x = 00100101011101010$

$z_1 = 00000000100001000$

$z_2 = 00000001000010000$

$t_0 t_1 t_2$

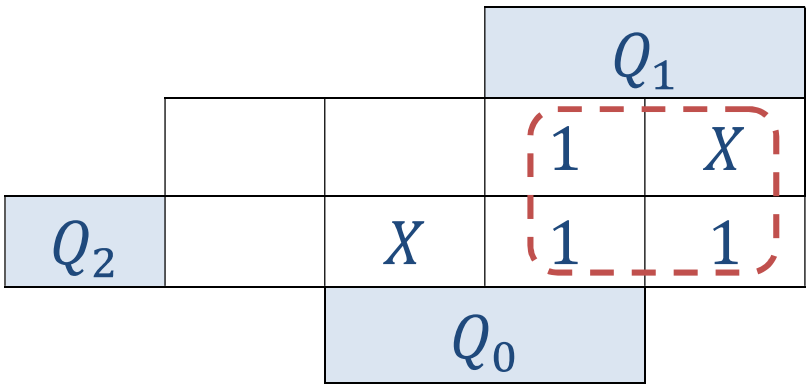
Prob.2: Design a counter with the following repeated binary 0, 1, 3, 7, 6, 4 using D-Flip-Flop.

Solution:

Counting tell 7 needs 3 bits

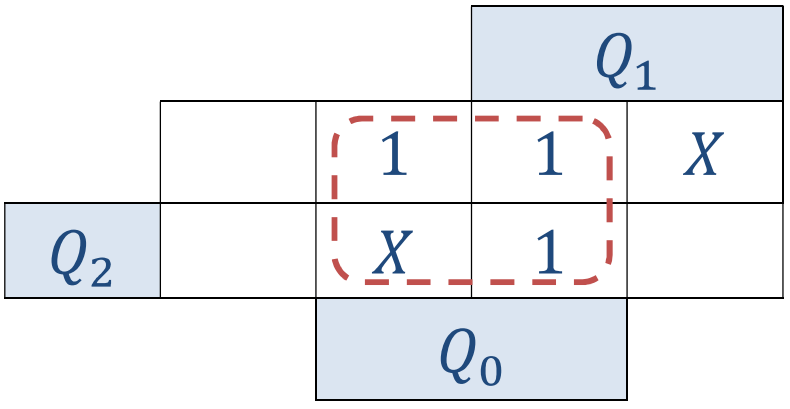
Present State			*Next State*		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	X	X	X
0	1	1	1	1	1
1	0	0	0	0	0
1	0	1	X	X	X
1	1	0	1	0	0
1	1	1	1	1	0

⇛ D_2:



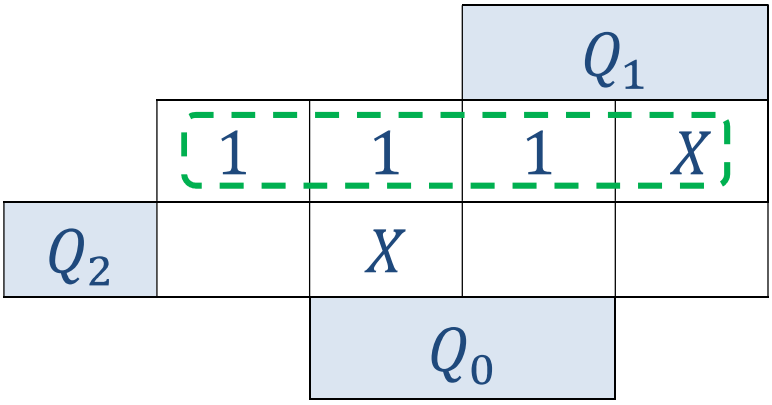
$D_2 = Q_1$

⇛ D_1:

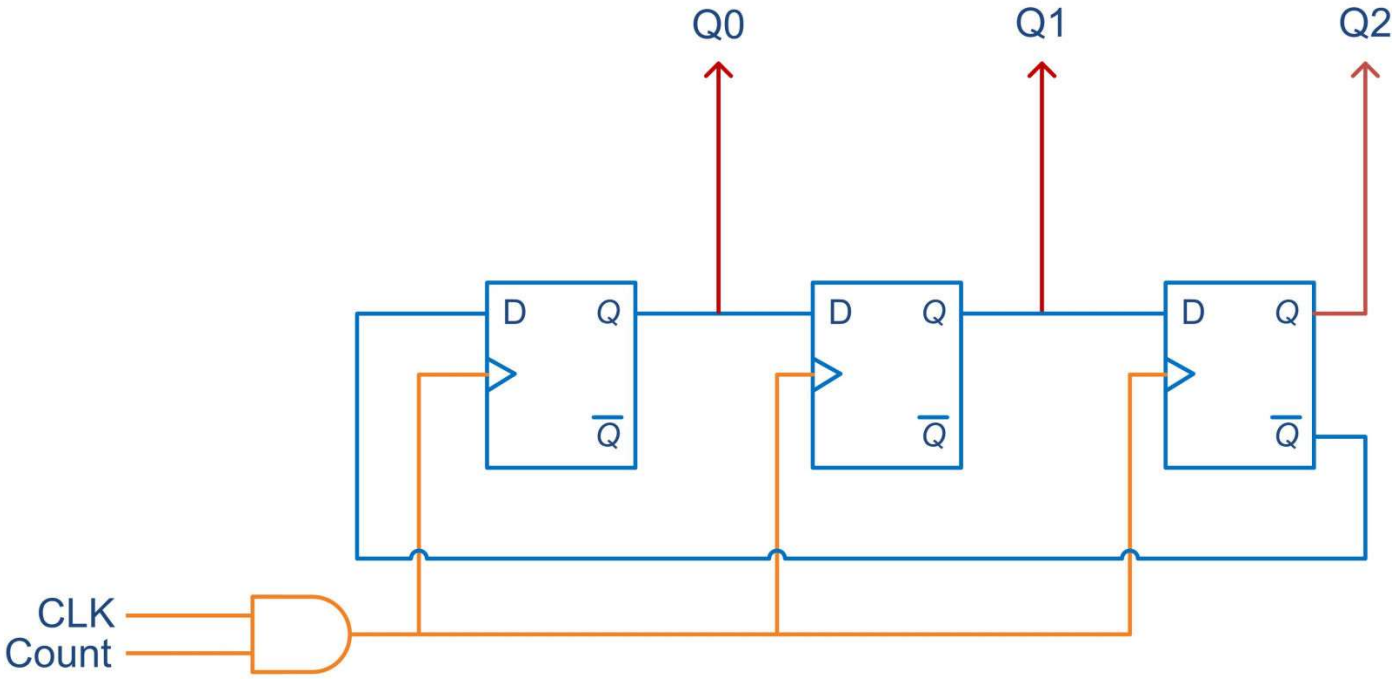


$D_1 = Q_0$

⇛ D_0:


Q_1
1
1
1
X
Q_2
X
Q_0

$D_0 = Q_2'$


Q0
Q1
Q2
D
Q
$\overline{Q}$
D
Q
$\overline{Q}$
D
Q
$\overline{Q}$
CLK
Count

Prob.3: Design an up/down 3-bit synchronous counter with JK-FFs.

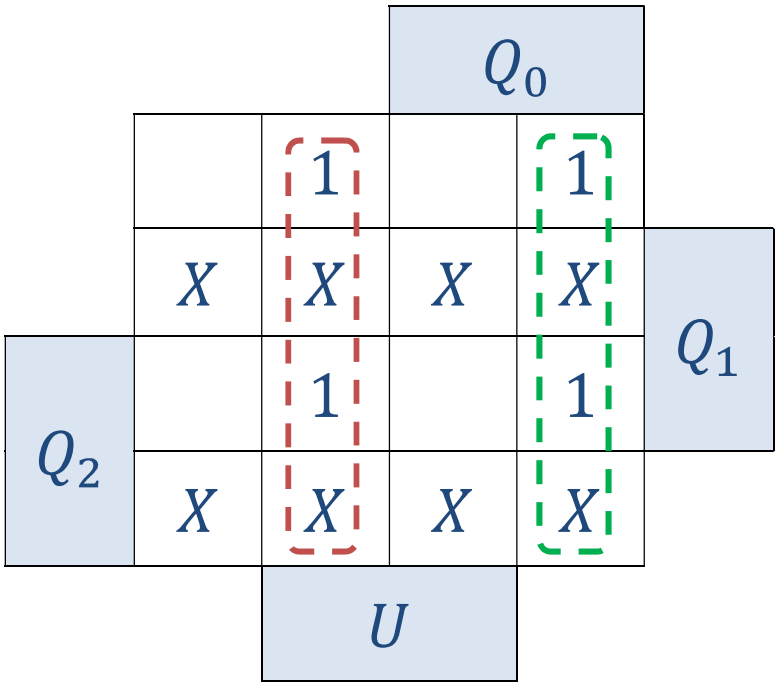
Solution:

$U = 0\ for\ up\ count, and\ 1\ for\ down.$

Present State			*I/P*	*Next State*			*Flip − Flops I/Ps*					
Q_2	Q_1	Q_0	U	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	0	1	0	X	0	X	1	X
0	0	0	1	1	1	1	1	X	1	X	1	X
0	0	1	0	0	1	0	0	X	1	X	X	1
0	0	1	1	0	0	0	0	X	0	X	X	1
0	1	0	0	0	1	1	0	X	X	0	1	X
0	1	0	1	0	0	1	0	X	X	1	1	X
0	1	1	0	1	0	0	1	X	X	1	X	1
0	1	1	1	0	1	0	0	X	X	0	X	1
1	0	0	0	1	0	1	X	0	0	X	1	X
1	0	0	1	0	1	1	X	1	1	X	1	X
1	0	1	0	1	1	0	X	0	1	X	X	1
1	0	1	1	1	0	0	X	0	0	X	X	1
1	1	0	0	1	1	1	X	0	X	0	1	X
1	1	0	1	1	0	1	X	0	X	1	1	X
1	1	1	0	0	0	0	X	1	X	1	X	1
1	1	1	1	1	1	0	X	0	X	0	X	1

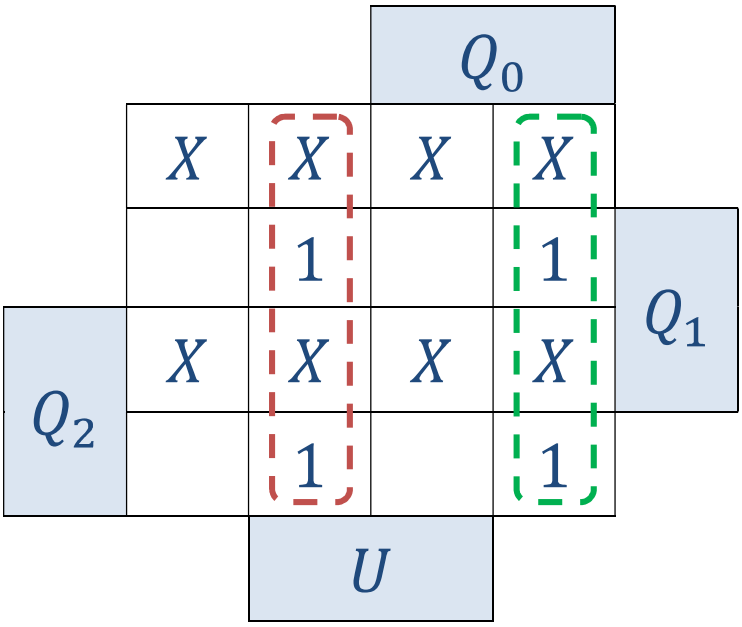
$J_0 = K_0 = 1$

⇛ J_1:



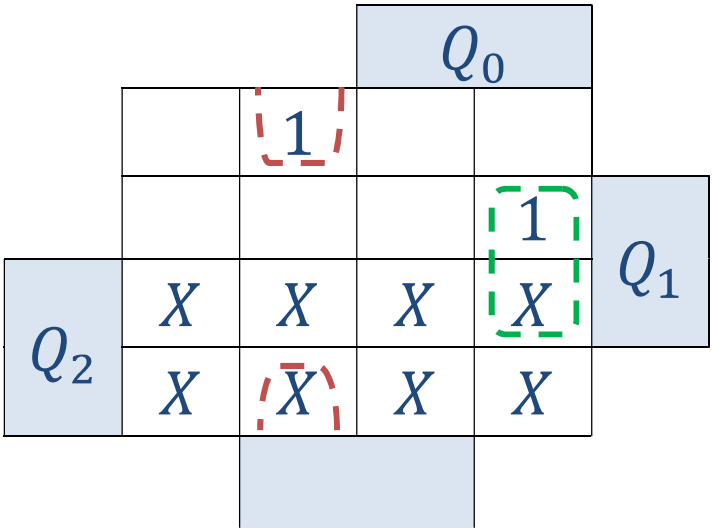
$J_1 = UQ_0' + U'Q_0$

⇛ K_1:



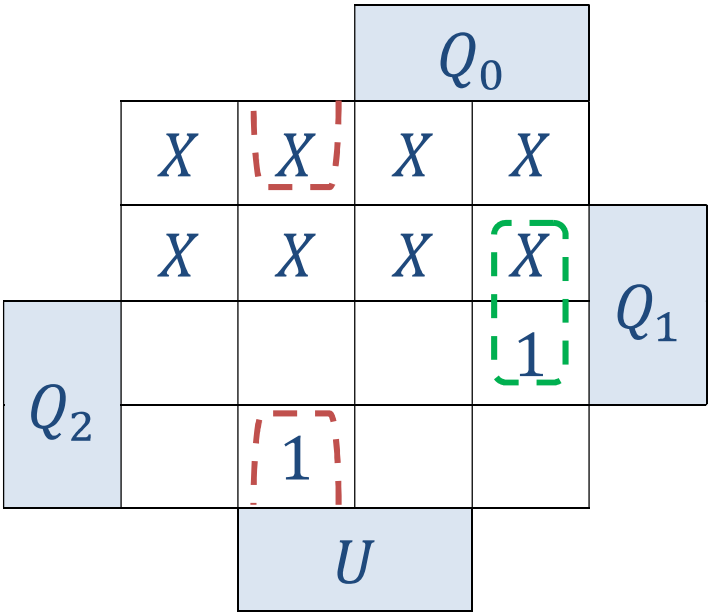
$K_1 = UQ_0' + U'Q_0$

⇛ J_2:

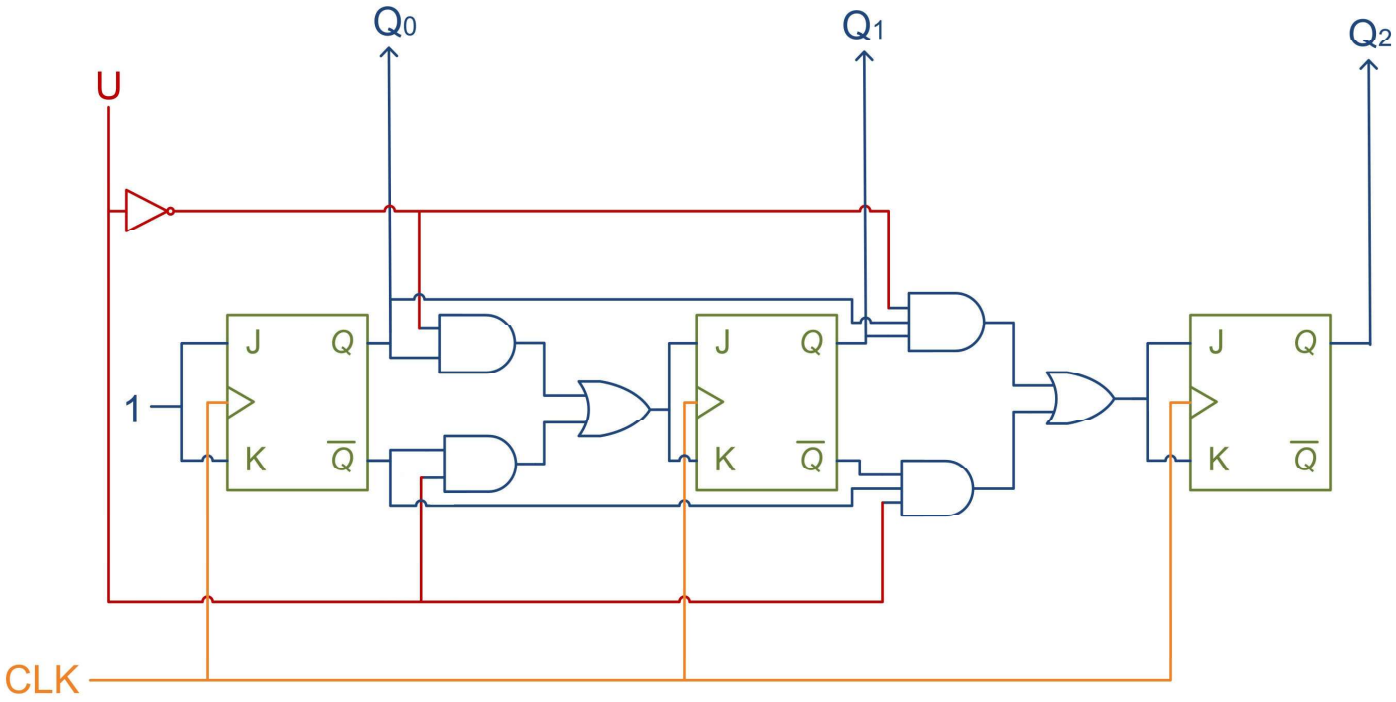


$J_2 = UQ_1'Q_0' + U'Q_1Q_0$

K_2:



$K_2 = UQ_1'Q_0' + U'Q_1Q_0$

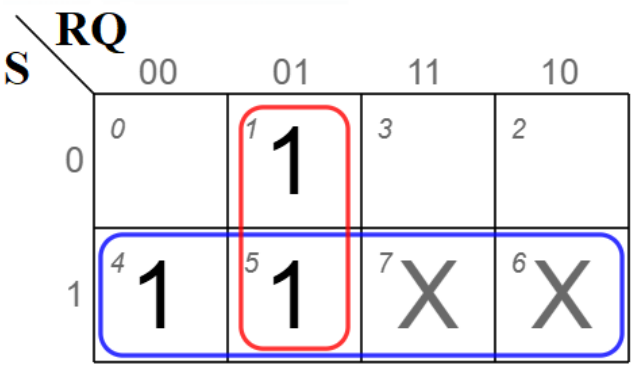

Q0
Q1
Q2
U
1
J
Q
K
Q
J
Q
K
Q
J
Q
K
Q
CLK

Problem # 09

Give the Characteristic equations and the Excitation tables for the *SR* and *JK* flip-flops.

Characteristic Table & Characteristic Equation of SR Flip-Flop

S	R	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-



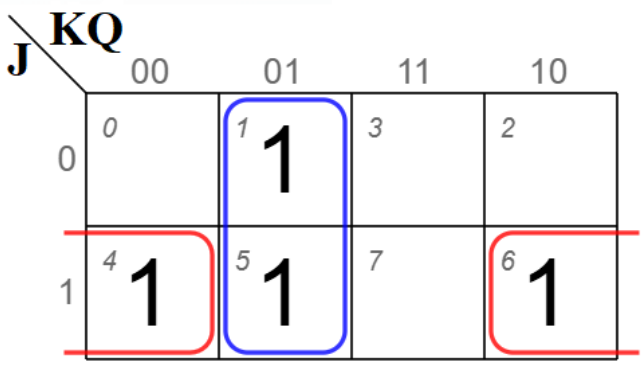
$$Q+ = S + R'Q$$

Excitation Table of SR Flip-Flop

Present State Q	Next State Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Characteristic Table & Characteristic Equation of JK Flip-Flop

J	K	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



$$Q+ = JQ' + K'Q$$

Excitation Table of JK Flip-Flop

Present State Q	Next State Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

The **next state** table for this state diagram *(1.5 marks)*

Input	Current State		Next State		Output
X	Q1	Q0	Q1	Q0	Y
0	0	0	1	1	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	0	0	1
1	1	0	1	1	0
1	1	1	0	1	0

The **excitation equations** if **J-K flip flops** are used to implement this state diagram (use the Karnaugh map in your solution).

J-K flip flop transition table: *(2 marks)*

$Q_{current}$	Q_{next}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Input	Current State		Next State		Output	flip flop inputs (excitation)			
X	Q1	Q0	Q1	Q0	Y	J1	K1	J0	K0
0	0	0	1	1	0	1	x	1	x
0	0	1	0	0	1	0	x	x	1
0	1	0	0	1	0	x	1	1	x
0	1	1	1	0	0	x	0	x	1
1	0	0	1	0	0	1	x	0	x
1	0	1	0	0	1	0	x	x	1
1	1	0	1	1	0	x	0	1	x
1	1	1	0	1	0	x	1	x	0

Karnaugh map *(2 marks)*

J1

XQ1 \ Q0	0	1
00	1	0
01	x	x
11	x	x
10	1	0

$J1 = \overline{Q0}$

K1

XQ1 \ Q0	0	1
00	x	x
01	1	0
11	x	x
10	0	1

$K1 = \overline{X}\,\overline{Q0} + XQ0$

J0

XQ1 \ Q0	0	1
00	1	x
01	1	x
11	1	x
10	x	0

$J0 = \overline{X} + Q1$

K0

XQ1 \ Q0	0	1
00	x	1
01	x	1
11	x	0
10	x	1

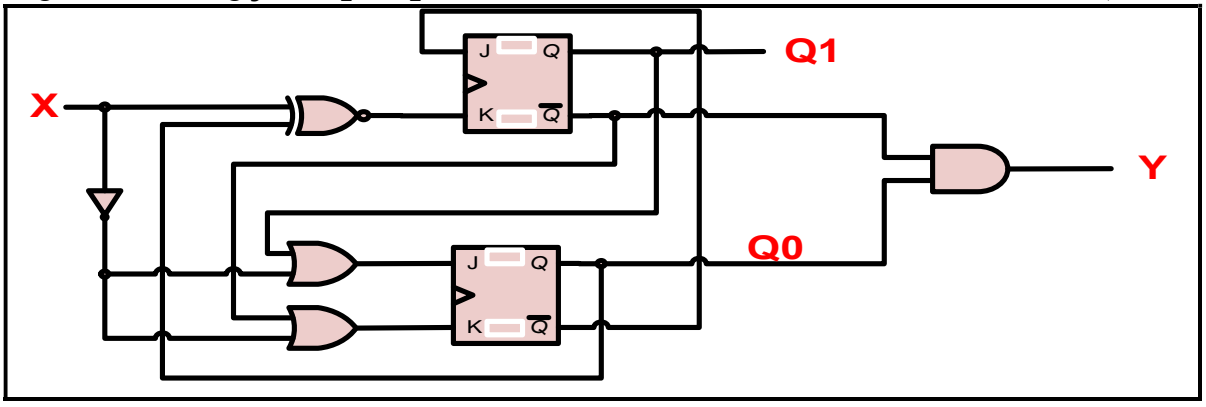
$K0 = \overline{X} + \overline{Q1}$

Y

XQ1 \ Q0	0	1
00	0	1
01	0	0
11	0	0
10	0	1

$Y = \overline{Q1}Q0$

The logic circuit using **J-K flip flops** *(1.5 marks)*

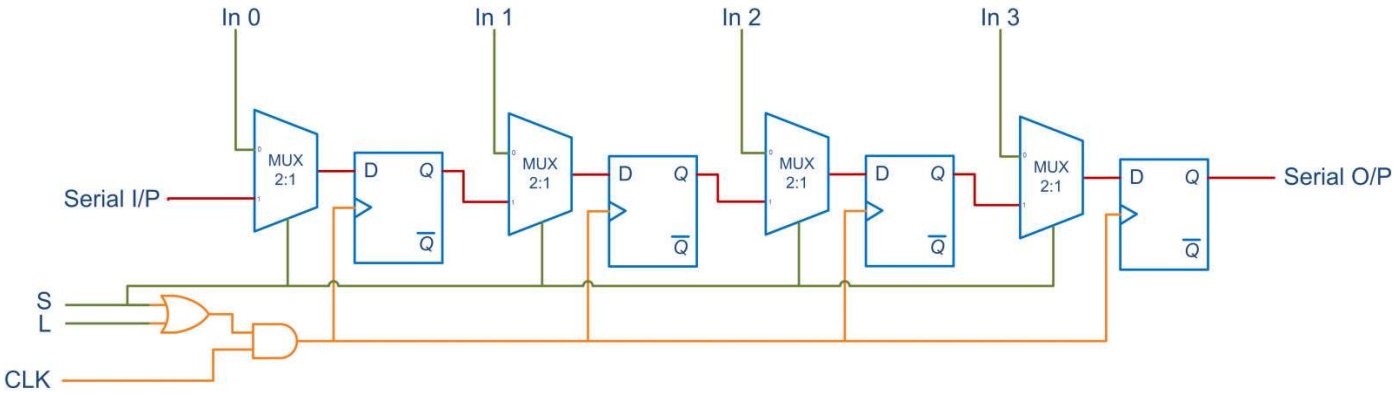


Sheet 12 – Solution

Prob.1: Design a 4-bit shift register with parallel load using D-FFs. There are two control inputs: shift and load. When shift =1, the content of the register is shifted by one position. New data is transferred into the register when load=1 and shift =0. If both control inputs are equal to 0, the content of the register doesn't change.

Solution:

S	L	*Operation*
1	X	$Shift$
0	1	$Load$
0	0	$No\ Change$



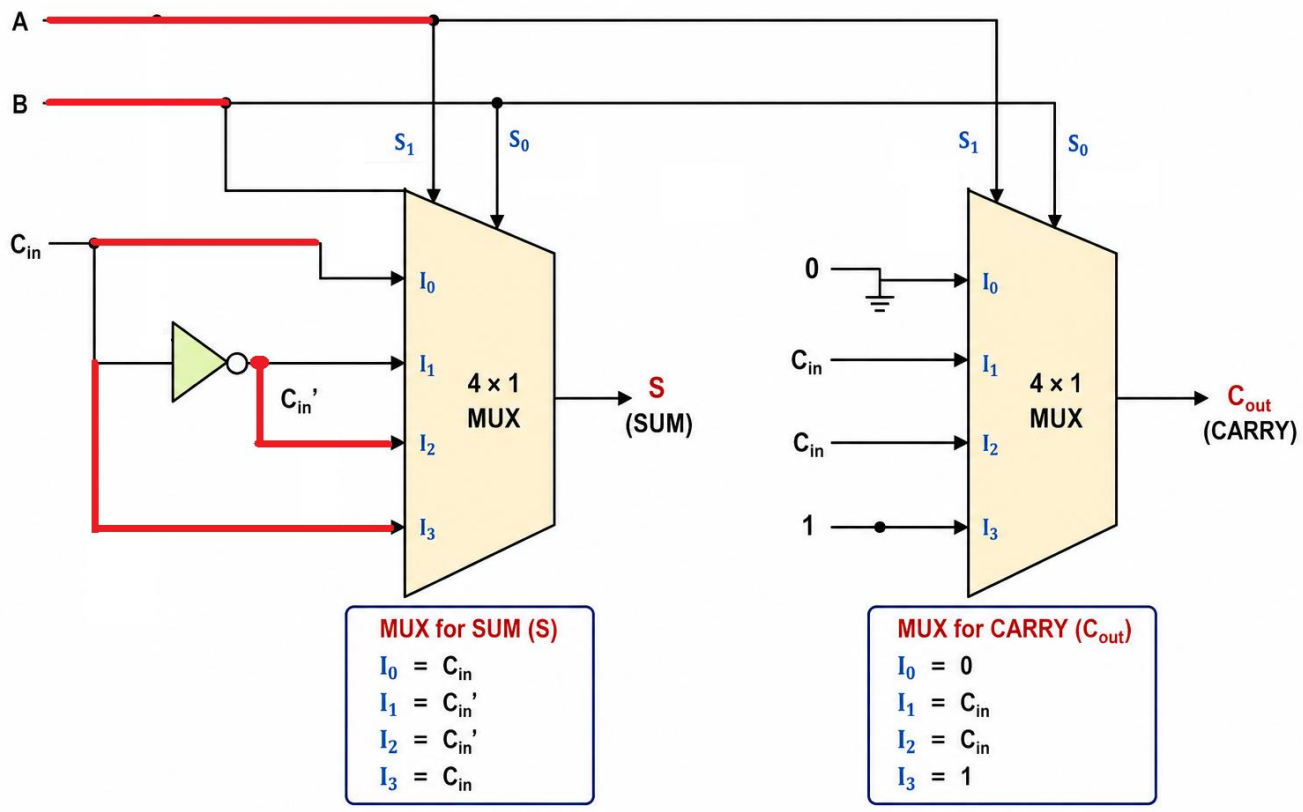
Note: passing clock through gates causes clock squing, and better not to be used.

Problem # 12 (4.33 Problem Digital Design by Morris Mano, 5th edition)

	S1 A	S0 B	Cin	S		Cout	
I0	0	0	0	0	Cin	0	0
	0	0	1	1		0	
I1	0	1	0	1	Cin'	0	Cin
	0	1	1	0		1	
I2	1	0	0	1	Cin'	0	Cin
	1	0	1	0		1	
I3	1	1	0	0	C	1	1
	1	1	1	1		1	

$$S = \sum(1, 2, 4, 7) \quad C_{out} = \sum(3, 5, 6, 7)$$

FULL ADDER USING TWO 4 × 1 MULTIPLEXERS



MUX for SUM (S)

$I_0 = C_{in}$
$I_1 = C_{in}'$
$I_2 = C_{in}'$
$I_3 = C_{in}$

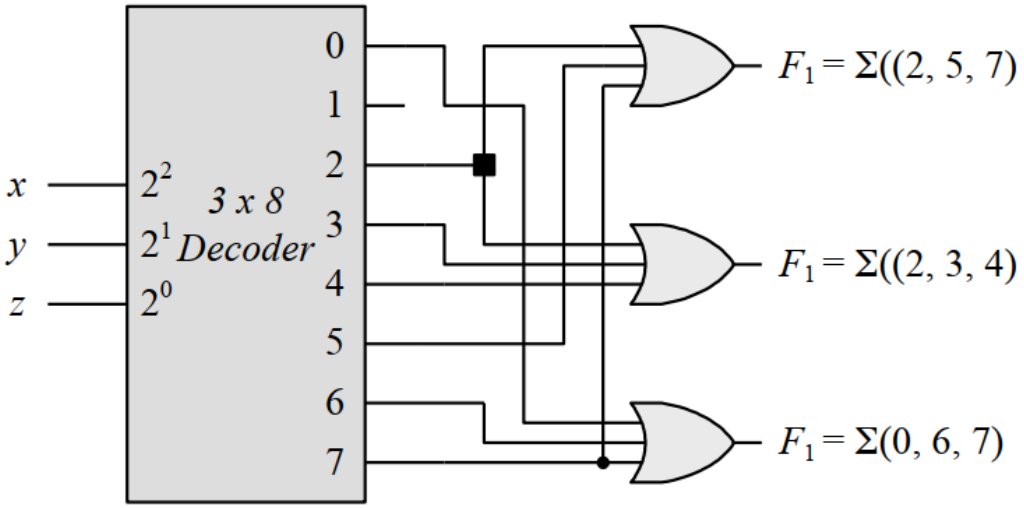
MUX for CARRY (C_{out})

$I_0 = 0$
$I_1 = C_{in}$
$I_2 = C_{in}$
$I_3 = 1$

Problem # 13 (4.28 Problem by Morris Mano)

(a)

$$F_1 = x(y + y')z + x'yz' = xyx + xy'z + x'yz' = \Sigma(2, 5, 7)$$
$$F_2 = xy'z' + x'y = xy'z' + x'yz + x'yz' = \Sigma(2, 3, 4)$$
$$F_3 = x'y'z' + xy(z + z') = x'y'z' + xyz + xyz' = \Sigma(0, 6, 7)$$

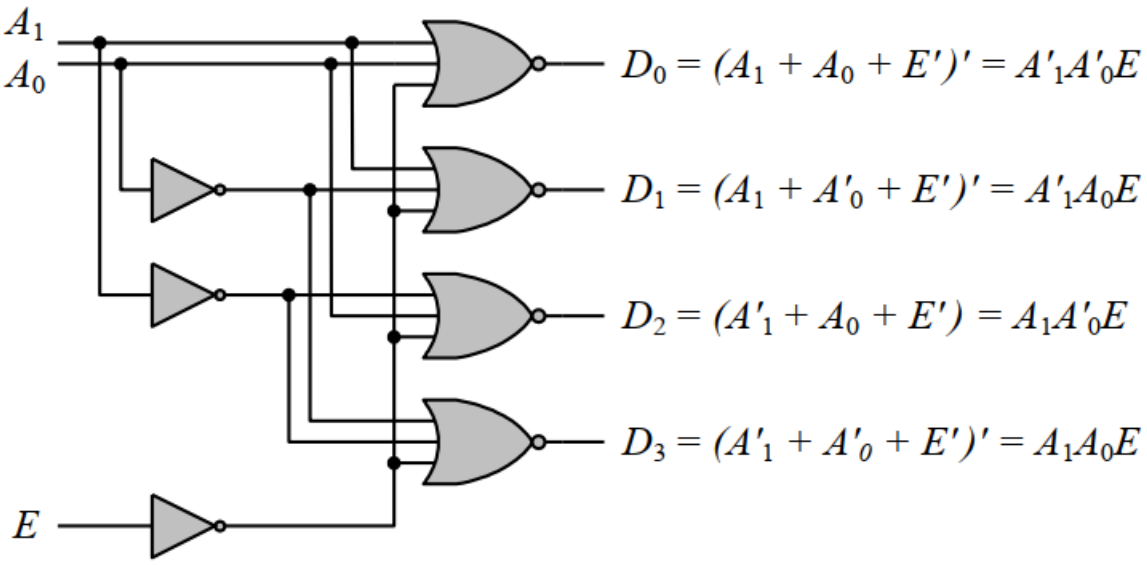


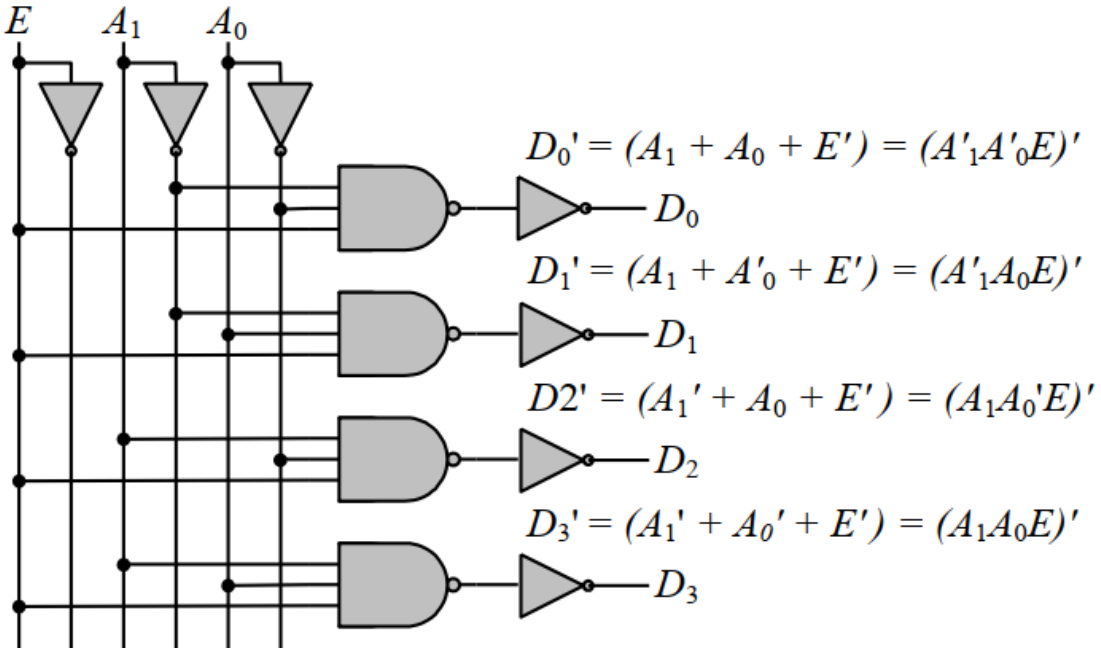
Part (b) do yourself

Problem # 14 (4.23 Problem by Morris Mano)

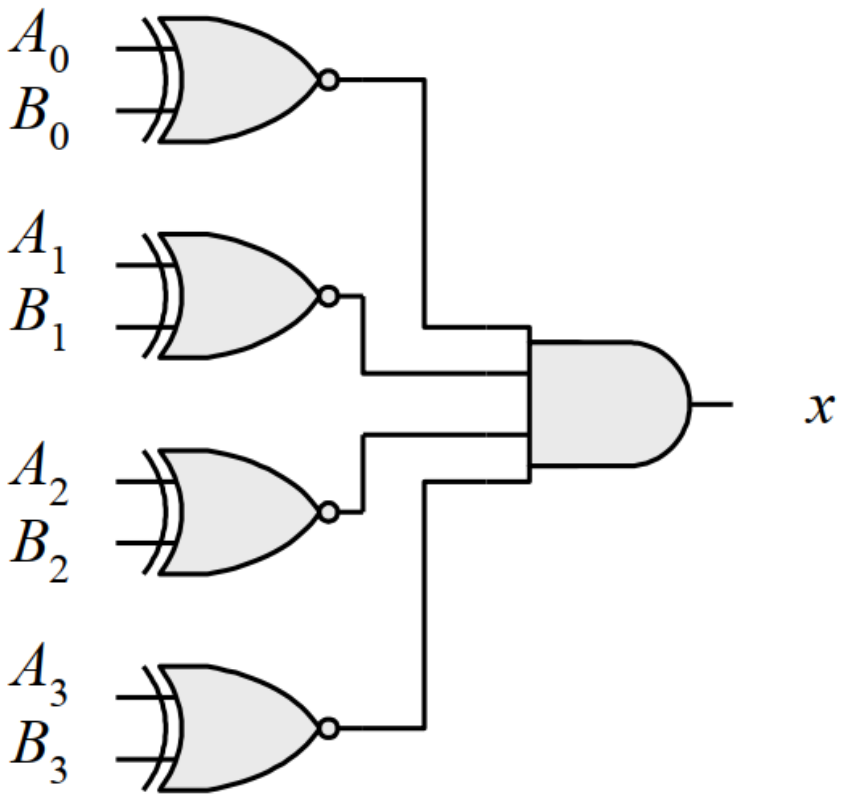
Draw the logic diagram of a 2-to-4-line decoder using (a) NOR gates only and (b) NAND gates only. Include an enable input.

D0 = A1'A0' = (A1 + A0)'	(NOR)	D0' = (A1'A0')'	(NAND)
D1 = A1'A0 = (A1 + A0')'	(NOR)	D1' = (A1'A0)'	(NAND)
D2 = A1A0' = (A1' + A0)'	(NOR)	D2' = (A1A0')'	(NAND)
D3 = A1A0 = (A1' + A0)'	(NOR)	D0' = (A1A0)'	(NAND)





Problem # 15 (4.21 Problem by Morris Mano)



$$x = (A_0 \oplus B_0)'(A_1 \oplus B_1)'(A_2 \oplus B_2)'(A_3 \oplus B_3)'$$

Bonus Problem

Complete the timing diagram of the following circuit. $Q = Q_3Q_2Q_1Q_0$. *[10 Marks]*