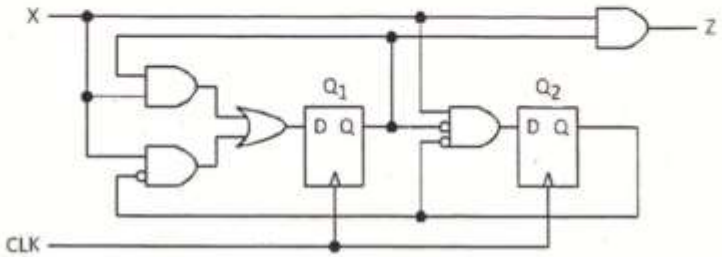
Problem # 01: What is Gated SR Latch? Or it circuit diagram maybe given, complete the truth table of SR latch. Is there any specific input combination for which we have an invalid output? If there, how can we get rid of this?

Problem # 02:

For the following clocked sequential circuit with one input (X) and one output (Z):

1. Drive a state table and draw a state diagram for the circuit.
2. Redesign this circuit by replacing the Q_1 flip-flop (i.e. the D flip-flop holding Q_1 state) with a JK flip-flop, and the Q_2 flip-flop with a T flip-flop. Only show the excitation equations (or state equations) for J_1, K_1, and T_2.



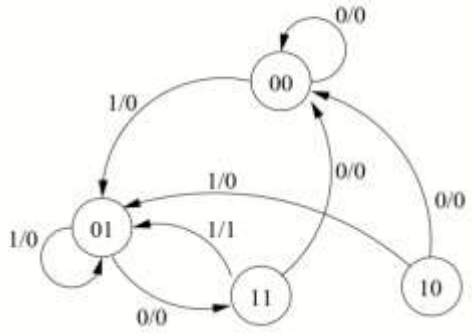
Problem # 03:

Draw the state diagram for the table below that describes a finite-state machine which has one input x and one output z.

Present State	Next State		Output (z)	
	x = 0	x = 1	x = 0	x = 1
A	A	E	1	0
B	C	F	0	0
C	B	H	0	1
D	E	F	0	0
E	D	A	0	1
F	B	F	1	1
G	D	H	0	1
H	H	G	1	0

Problem # 04:

Consider the following state diagram for a synchronous circuit with one input X and one output Z. Analyze this state diagram and draw its circuit implementation using JK flip-flop (state Q0) and T flip-flop (state Q1) and MUX-4x1 for Z.



Problem # 05:

Design a digital circuit that takes two 4-bit numbers A and B as input and generates output Z as follows:

- If A and B are odd numbers then Z=A-B
- If A and B are even numbers then Z=B-A
- If A is an even number and B is an odd number then Z=A+B
- If A is an odd number and B is an even number then Z=A-B-1

Assume that you have access to as many as you need of AND, OR, INV, XOR gates and only one FULL-ADDER, DECODER and MULTIPLEXER of any size.

Problem # 06:

Draw a circuit diagram for non-overlapped '101' detector with "D" flip-flops as a Mealy and Moore machine.

Problem # 07:

Design a counter with the following repeated binary 0, 1, 3, 7, 6, 4 using D-Flip-Flop.

Problem # 08:

Design an up/down 3-bit synchronous counter with JK-FFs.

Problem # 09:

Give the Characteristic equations and the Excitation tables for the *SR* and *JK* flip-flops

SR flip-flop

$$Q+ = S + R'Q$$

S	R	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	-
1	1	1	-

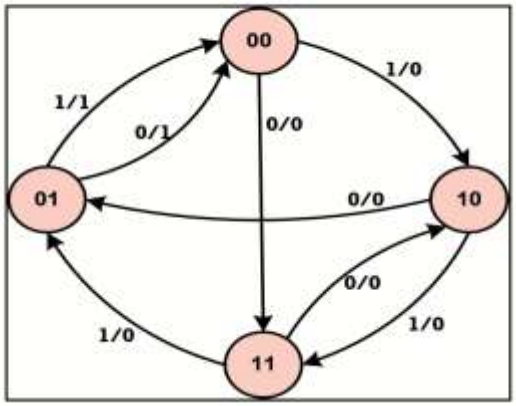
JK flip-flop

$$Q+ = JQ' + K'Q$$

J	K	Q	Q+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Problem # 10:

Given the following **state diagram**, design a clocked sequential circuit using **JK flip-flops**.



Problem # 11:

Design a 4-bit shift register with parallel load using D-FFs. There are two control inputs: shift and load. When shift =1, the content of the register is shifted by one position. New data is transferred into the register when load=1 and shift =0. If both control inputs are equal to 0, the content of the register doesn't change.

Problem # 12:

Implement a full adder with two 4 × 1 multiplexers.

Problem # 13:

Using a decoder and external gates, design the combinational circui defined by the following three Boolean functions:

(a) $F_1 = x'yz' + xz$
$F_2 = xy'z' + x'y$
$F_3 = x'y'z' + xy$

(b) $F_1 = (y' + x)z$
$F_2 = y'z' + x'y + yz'$
$F_3 = (x + y)z$

Problem # 14:

Draw the logic diagram of a 2-to-4-line decoder using (a) NOR gates only and (b) NAND gates only. Include an enable input.

Problem # 15:

Design a combinational circuit that compares two 4-bit numbers to check if they are equal. The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.